First name: Alan Rodrigo Last name: DIAZ RIZO

Email: alan-rodrigo.diaz-rizo@lip6.fr
Google scholar: Alán R. Díaz Rizo
LinkedIn: /alandr9
ORCiD: 0000-0003-2849-8122
Place of residence: Paris, France
Phone: +33 6 09 88 63 05
Office: Faculté des Sciences et Ingénierie, Sorbonne Université, LIP6

Research interests

Hardware Security, Anti-piracy design, Intellectual Property (IP) protection for Integrated Circuits (ICs), Hardware Trojans (HT), RF transceivers, Telecommunications

Current position

Sorbonne Université, CNRS, LIP6 — Paris, France
Post-doctoral researcher — Oct 2023 – Present

Education

Sorbonne Université, CNRS, LIP6 — Paris, France
Ph.D. — Oct 2019 – Jan 2023
Field: Computer Science, Telecommunications and Electronics
Advisors: Professors Haralampos Stratigopoulos, Hassan Aboushady
Title: Security and Trust for Wireless Integrated Circuits. Available here.

Center for Research and Advanced Studies of the NPI (Cinvestav - Guadalajara) — Zapopan, Mexico
M.Sc. in Electrical Engineering — Sep 2016 – Dec 2018
Field: Telecommunications
Advisor: Professor Ramón Parra Michel
Title: Characterization, modeling, estimation and compensation techniques for widely linear systems in software-defined radios with homodyne transceivers.

University of Guadalajara (UDG) — Guadalajara, Mexico
B.Sc. in Electronics and Communications Engineering — Aug 2010 – Dec 2015

Internships

Sorbonne Université, CNRS, LIP6 — Paris, France
Research Internship — Jun 2018 – Sep 2018
Objective: Development of calibration algorithms for a software-defined radio platform to enable it with spectrum sensing capability.

Exchanges

National Institute of Applied Sciences (INSA) — Toulouse, France
Fourth year of Electrical and Information Engineering — Sep 2014 – Jun 2015

Research experience

Sorbonne Université, CNRS, LIP6 — Paris, France
Post-doctoral researcher — Oct 2023 – Present
Objective: Research and development of techniques to prevent intellectual property theft of RF integrated circuits based on patented technology.
- Research performed during CNRS pre-maturation project *SyncLock*. Project information available here (p. 68).

Sorbonne Université, CNRS, LIP6 — Paris, France
Research Engineer — Feb 2023 – Sep 2023
Objective: Anti-piracy design of RF transceivers.
Result 1: Dataset generation for covert communication channel detection.
Result 2: Dataset generation for RF jamming classification.

Sorbonne Université, CNRS, LIP6 — Paris, France
Ph.D. candidate researcher — Oct 2019 – Jan 2023
Objective: Research and development of hardware security mechanisms to protect wireless communication devices against Intellectual Property (IP) theft, Integrated Circuit (IC) piracy, hardware Trojan infection, and unauthorized use.
- Summary of findings available here.

Cinvestav and UPMC — Mexico and France
M.Sc. candidate researcher — Sep 2017 – Dec 2018
Mentors: Professors Ramón Parra Michel and Hassan Aboushady
- Research performed during M.Sc., project summary available here.

Fellowship & Grants

Pre-maturation program (CNRS - France) 2023
Ph.D. fellowship (CONACYT - Mexico) 2019
Exchange grant (CONACYT - Mexico) 2018
M.Sc. fellowship (CONACYT - Mexico) 2016
MEXFITEC fellowship (SEP - Mexico) 2014

Awards

Best Thesis Award (2nd) (Doctoral School EDITE) 2022
Laureate of the innovation contest i-PhD (Bpifrance) 2022
Project name: SyncLock. 2022 Awards here.

Contests

Falling Walls Lab Paris (pitch contest) - contestant 2023
"Breaking the wall of Integrated Circuit piracy and IP theft"

Training

Deeptech Founders — Oct 2022 - Jul 2023
Program to help entrepreneurial scientists and engineers explore opportunities to transform their research into a commercial product.
Ticket for Change — Oct 2022 - Jul 2023
Training in entrepreneurship and individual skills development.
Adoc Talent Management — Oct 2022 - Jul 2023
Recruitment consulting firm specialized in the recruitment and career development of PhDs.

Professional Service

Computers & Security — Scientific Journal
Reviewer on Hardware Security topics — Since 2022

Cinvestav - Guadalajara — Zapopan, Mexico
Position: Design Engineer — Jan 2019 - Aug 2019
Department: Telecommunications laboratory
Mission: Logic IP cores design engineering.

Teaching Responsibilities

Sorbonne Université — Paris, France
Department: UFR 919 of Engineering
Position: Teaching assistant

Master 2: Advanced Analog Circuit Design	
	TD (4h) 2023-2024
	TD (10h) 2020-2021
Master 1: Summer Scientific Internship	
	Internship Co-tutor 2022-2023
Master 1: SESI project	
	TD (12h) 2022-2023
Licence 3: Digital Systems and Embedded Processors	
	TP (16h) 2023-2024
	TP (16h) 2022-2023
	TP (16h) 2021-2022
	TP (16h) 2020-2021
Licence 2: Analog and Digital Electronics	
	TP (20h) 2023-2024
	TP (20h) 2022-2023
	TP (20h) 2021-2022
Licence 2: Digital, Combinatorial and Sequential Electronics	
	TP (20h) 2020-2021

Panamerican University — Guadalajara, Mexico
Department: DFA
Position: Tutor

Subjects/Fields: Linear algebra, calculus, and trigonometry	2017-2018

Publications: Peer-Reviewed Journal Articles

First author

1. **Leaking Wireless ICs via Hardware Trojan-Infected Synchronization**
   A. R. Díaz-Rizo, H. Aboushady, H.-G. Stratigopoulos
   IEEE Transactions on Dependable and Secure Computing, vol. 20, no. 5, pp. 3845-3859, 1 Sept.-Oct. 2023, doi: 10.1109/TDSC.2022.3218507. HAL.

2. **Anti-Piracy Design of RF Transceivers**
   A. R. Díaz-Rizo, H. Aboushady, H.-G. Stratigopoulos
   IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 1, pp. 492-505, Jan. 2023, doi: 10.1109/TCSI.2022.3214111. HAL.

3. **RF Transceiver Security Against Piracy Attacks**
   A. R. Díaz-Rizo, J. Leonhard, H. Aboushady, H.-G. Stratigopoulos
   IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 7, pp. 3169-3173, July 2022, doi: 10.1109/TCSII.2022.3165709. HAL.

Co-author

1. **Digitally Assisted Mixed-Signal Circuit Security**
   J. Leonhard, N. Limaye, S. Turk, A. Sayed, A. R. Díaz-Rizo, H. Aboushady, H.-G. Stratigopoulos
   IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 41, no. 8, pp. 2449-2462, August. 2022, doi: 10.1109/TCAD.2021.3111550. HAL.

2. **Tunable filtenna with DGS loaded resonators for a cognitive radio system based on an SDR transceiver**
   A. A. Ibrahim, H. A. Mohamed, A. R. Díaz-Rizo, R. Parra-Michel, H. Aboushady
   IEEE Access, vol. 10, pp. 32123-32131, 2022, doi: 10.1109/ACCESS.2022.3160467. Open Access.

Publications: Conference Papers

First author

1. **SyncLock: RF transceiver security using synchronization locking**
   A. R. Díaz-Rizo, H. Aboushady, H.-G. Stratigopoulos
   2022 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, 2022, pp. 1153-1156, doi: 10.23919/DATE54114.2022.9774556. HAL.

2. **Técnicas de optimización de algoritmos digitales a implementarse en VLSI: Aplicación a un filtro en celosía** (Optimization techniques for digital algorithms to be implemented in VLSI: Application to a lattice filter)
   A. R. Díaz-Rizo, A. Pérez-Haro y J. Rivera-Domínguez
   Coloquio en Electronica Analogica y Digital (COLEAD), 2017.

Publications: Thesis

1. **Security and Trust for Wireless Integrated Circuits**
   A. R. Díaz-Rizo
   Cryptography and Security. Sorbonne Université, Jan. 2023. ⟨NNT : 2023SORUS005⟩. ⟨tel-03941314v3⟩

Publications: Patents

1. **Method for securing telecommunication transceiver integrated circuit designs against piracy, counterfeiting and unauthorized use**
   H.-G. Stratigopoulos, A. R. Díaz-Rizo, H. Aboushady
   International Application No. PCT/IB2022/000135 Mar 2022
   Publication Number: WO/2023/170439 Sep 2023

Presentations: Workshops, Talks and tutorials

Public speaker: A. R. Díaz-Rizo

1. **Covert Communication Channels based on Hardware Trojans: Open-Source dataset generation and AI-based detection**
   Conference: Journée Thématique GDR SoC^2
   Place and date: Paris, France. Nov 2023
   Workshop: Hardware security and open-source

2. **Hardware security for integrated circuits**
   Conference: Electronics, Automation and Communications Congress 2023
   Place and date: Monterrey, Mexico. Nov 2023

3. **Security and trust for Wireless Integrated Circuits**
   Place and date : Cinvestav - Guadalajara, Zapopan, Mexico. Jun 2023

4. **RF Transceiver Security using Synchronization Locking**
   Conference: Design, Automation & Test in Europe (DATE 2022)
   Place and date: Anvers, Belgium. Mar 2023
   Workshop: Defense Techniques for Secure and Trustworthy Systems

5. **Hardware security and trust for RF transceivers**
   Conference: European Microwave Week 2022 (EuMW 2022)
   Place and date: Milan, Italy. Sep 2022
   Workshop: RF and mmW reliable ICs: characterization, test and security challenges

6. **Anti-Piracy Security for RF Transceivers**
   Conference: Colloque GDR SoC^2 (CGDR 2022)
   Place and date: Strasbourg, France. Jun 2022

Skills: Foreign languages

Spanish (Native)
English (Full Professional Proficiency)
French (Full Professional Proficiency)